

REDUCED SIZE AND POWER DEMAPPER FOR VITERBI DECODING

Joseph Paul Lauer

Alan Corry

ABSTRACT OF THE DISCLOSURE

[054] A Viterbi decoding demapping scheme for a wireless communications device processor substantially implemented on a single CMOS integrated circuit is described. By using log and antilog techniques, simplified multiplication and division operations in the branch metric calculation may be performed. A fully integrated receiver circuit with Viterbi decoder with branch metric computation consumes less circuit space and power than conventional solutions.